

**IN THE SPECIFICATION:**

Please replace the section “Brief Summary of the Invention” beginning on page 5, (paragraphs [17] – [19] of the specification) with the following replacement section:

- [17] According to an aspect of the present invention, there is provided a semiconductor device comprising a memory cell array having NAND cells arranged therein, a plurality of latch circuits which temporarily hold data read out from the memory cell array, a first circuit configured to generate a first current varying in proportion to “1” or “0” of binary logic data of one end of the plurality of latch circuits, a second circuit configured to generate a second current which is preset, and a third circuit configured to compare the first current with the second current wherein the value of “1” or “0” of binary logic data of the one end of the plurality of latch circuits is detected based on a result of the comparison between the first current and the second current.